Narrow VDC Extended Battery Life (EBL) Technique Battery Pack Specification for Intel Customer Reference Boards

Specification

December 2003

Order Number: 300344-001

Contents

Figures

Tables

Revision History

Rev.	Document Number	Description	Date
-001	300344	Initial Release	December 2003

1. Overview

The battery pack in this specification will be used to provide power while evaluating Intel development platforms. It is based on a traditional smart battery configuration; two additional control pins (CHR and DIS#) are added to support some new features. The pack is constructed of six, 18650 Li-Ion cells connected in a 3S2P configuration. The conventional battery monitoring board must be modified to accommodate the new pins and the additional control circuitry.

1.1. Electrical Design

Figure 1. Conventional Battery Pack

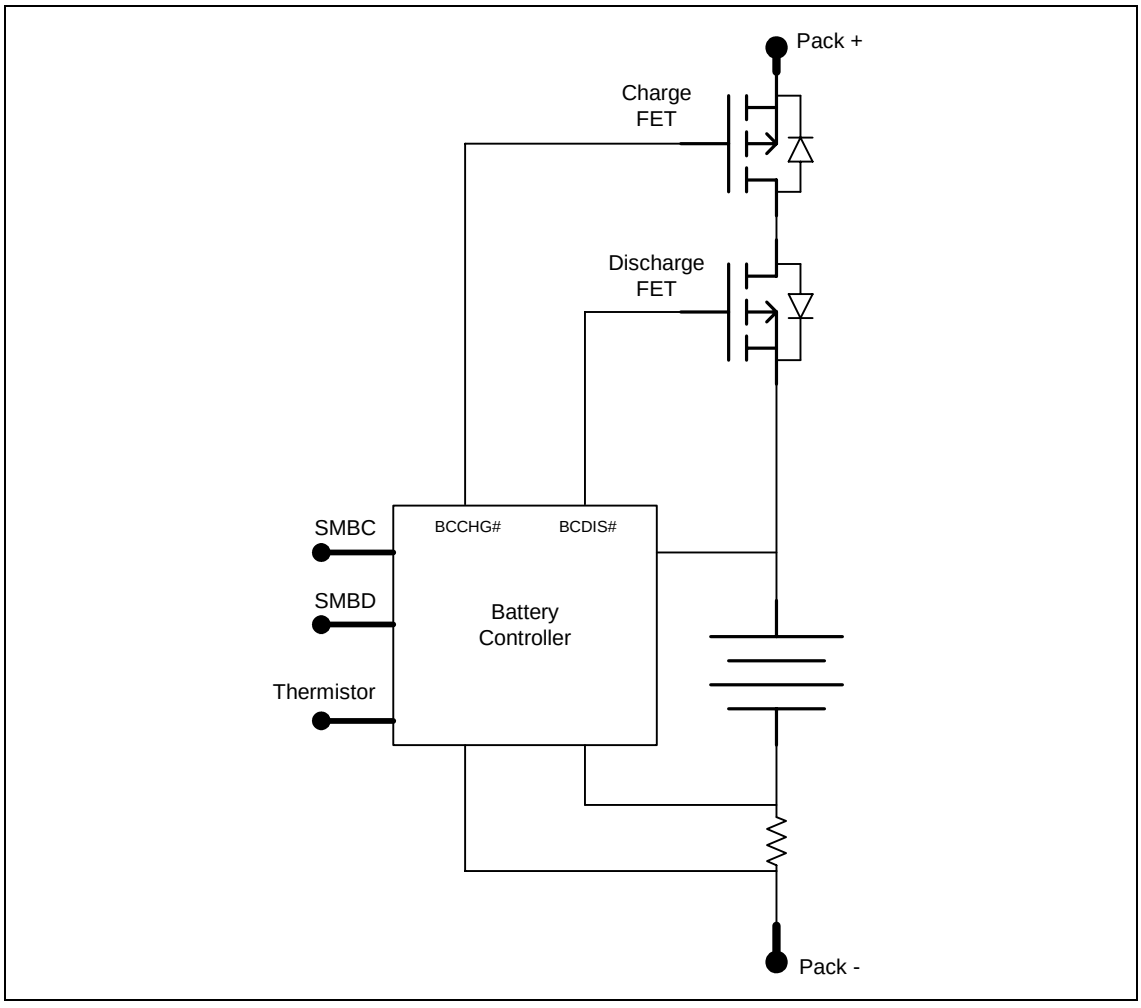
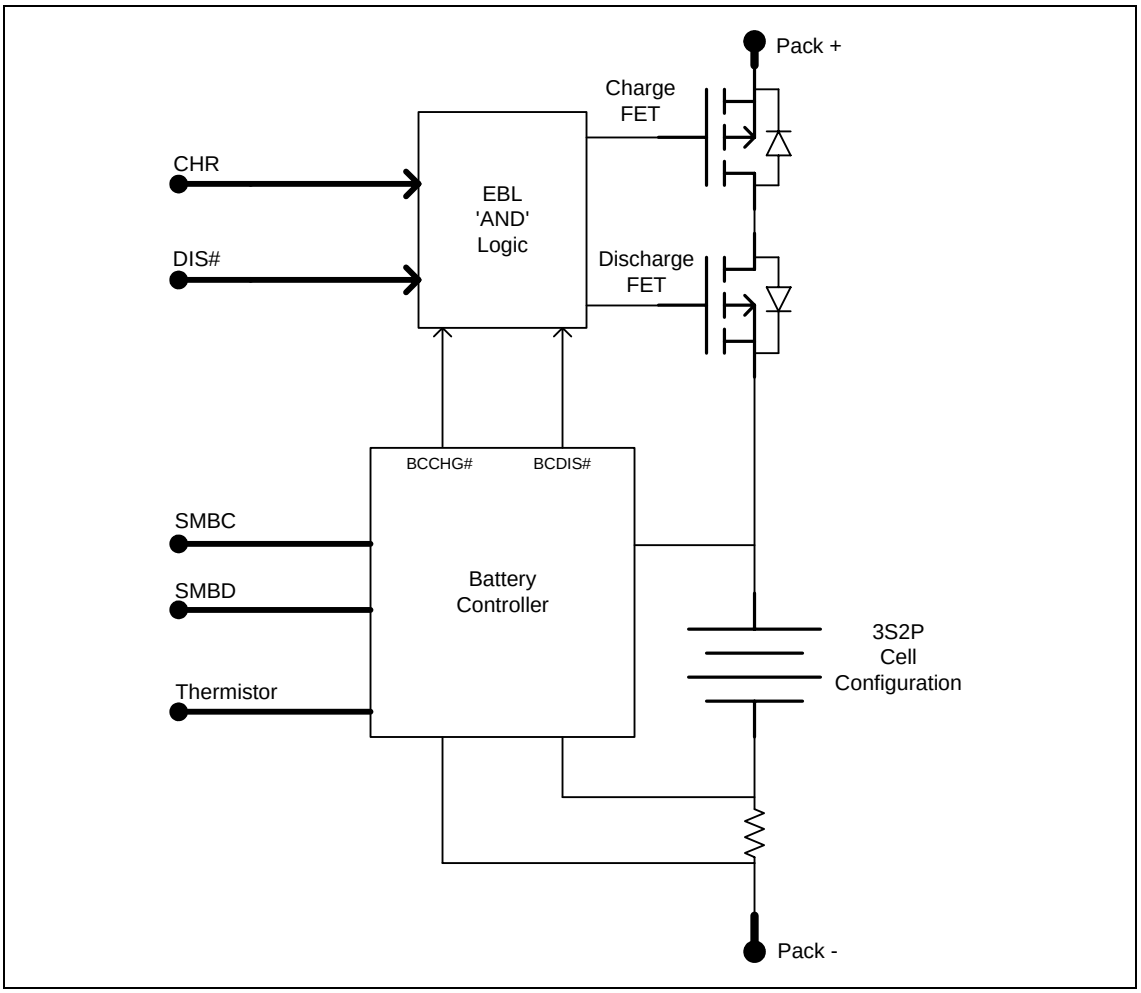


Figure 2. Modified Battery Pack



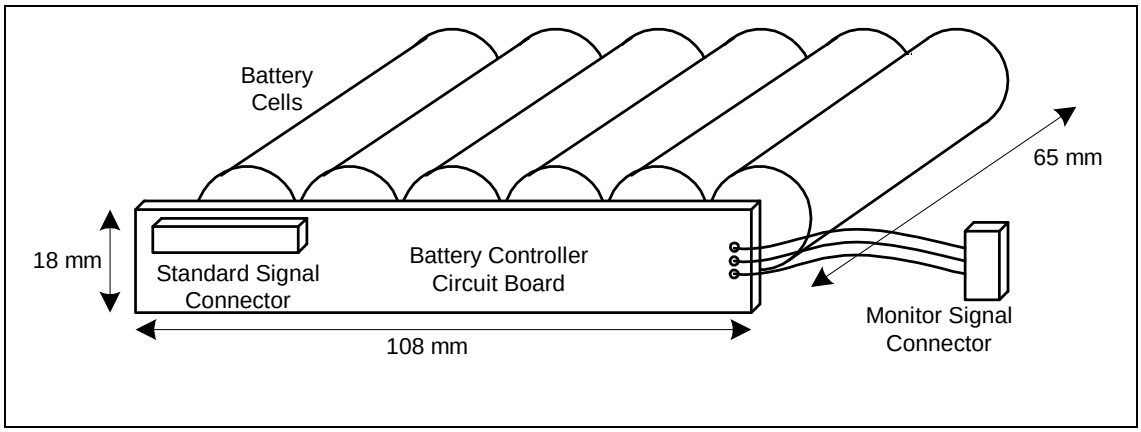
The representative circuits in Figure 1 and Figure 2 show P-Channel FETs used for the power switches. The battery pack could also be constructed using N-Channel FETs, the choice is left to the battery pack vendor.

1.2. Mechanical Design

The mechanical design specifications are a recommendation and are subject to change based upon discussions with battery pack vendors.

The battery cells can be placed side-by-side, forming a rectangular brick approximately 18-mm thick, 65-mm wide, and 108-mm long. The battery controller board dimensions can be up to 18 mm by 108 mm and placed along one end of the battery cells. A seven-pin connector should be used to provide connections for the traditional battery pack signals (Pack+, Pack-, Thermistor) and the two new control signals (CHR and DIS#).

Figure 3. Battery Pack Mechanical Design



1.3. Functional Description

1.3.1. Pack+, Pack-, SMBC and SMBD Pins

The Pack+, Pack-, SMBC, and SMBD pins that are found on conventional battery packs will function in the traditional manner. The SMBC and SMBD pins will be used for the SMBus clock and SMBus data signals respectively. The Pack+ pin will provide the positive voltage from the pack and the Pack- pin will supply the negative voltage from the pack.

1.3.2. CHR and DIS# Pins

The CHR and DIS# pins are used to allow the motherboard to control the power FETs located in the battery pack; the controller in the battery pack will still also have the ability to control the power FETs located in the battery pack. This added functionality eliminates the need for power path selector and battery charge selector switches on the motherboard. The elimination of the switches will reduce the cost and increase the power delivery efficiency of the motherboard design.

The CHR and DIS# pins are 3.3-V logic compatible; the functions of these signals are defined in Table 1. The motherboard signals perform a logical AND operation with the corresponding battery controller functions; either the motherboard signal or the battery controller signal can disable the battery pack FET.

Table 1. CHR and DIS# Signal Functions

Signal				FET		Comments
CHR	DIS#	BCCHR#	BCDIS#	CHARGE	DISCHARGE	
1	0	0	0	ON	ON	Battery is connected with both FETs ON
0	0	X	0	OFF	ON	Battery can only be discharged; through body diode of Charge FET
X		1				
1	1	0	X	ON	OFF	Battery can only be charged; through body diode of Discharge FET
	X		1			
0	1	X	X	OFF	OFF	Battery is isolated with both FETs OFF
X	X	1	1			

1.3.3. SMBus Address Selection

The thermistor pin will be used to set the SMBus address for the battery pack. This feature is required in order to use multiple battery packs in systems without the need for a separate SMBus for each battery pack. A resistor will be placed on the motherboard between the thermistor pin and ground. The circuitry on the battery pack controller board will have the ability to detect the value of the resistor and set the SMBus address in accordance with the values in Table 2. For this application only, addresses 16 and 20 will be used.

Table 2. SMBus Address Resistor Values

SMBus Address Resistor Values (Ohms, 5% tolerance)		SMBus Address
Host Resistor	Total Resistance (Host + 200 ohms ESD protection)	
820	1020	14
1800	2000	16
2700	2900	18
3900	4100	1A
4700	4900	1C
6800	7000	1E
9100	9300	20
11000	11200	22

2. Specifications

Table 3. Standard Signal Pin Definitions

Pin #	Pin Name	Pin Type	Pin Description
1	Pack+	PWR	Battery pack power – positive
2	SMBC	I/O, digital	SMBus – clock
3	SMBD	I/O, digital	SMBus – data
4	Thermistor	I, analog	Resistor to ground on motherboard, sets SMBus address for pack
5	Pack-	PWR	Battery pack power – negative
6	CHR	I, digital	Charge FET enable; 3.3-V logic compatible
7	DIS#	I, digital	Discharge FET enable; 3.3-V logic compatible

Table 4. Battery Pack Specifications

Parameter	Value	Comments
Application	Notebook PC	
Cell type	18650 Li-Ion	
Cell capacity	2400 mAh	Maximum available cell capacity is desired
Number of cells	6	
Cell configuration	3S2P	
Gas gauge	Yes	
Discharge time	5.3 hours	
Discharge requirement - average	10 W	0.9 A at 11 V
Discharge requirement - peak	50 W	5.75 A at 8.7 V
Termination voltage	8.7 V	2.9 V per cell
Operating temperature	Laboratory environment	
Storage temperature	Laboratory environment	
Charging conditions	CC-CV	Suggestion is 4.8 A maximum charge current
Package material	TBD	
Weight	TBD	
Dimensions	Approx. 25 mm x 70 mm x 115 mm	Dimensions do not include protrusions for connectors
Mechanical mounting	TBD	Method to secure battery pack to evaluation board or chassis
Safety standards	TBD	Will be used by OEMs and ODMs for product development purposes

Parameter	Value	Comments
Connector – power and control	AMP – 1318574-4 or similar	Pack+, Pack-, SMBC, SMBD, Thermistor, CHR#, DIS#